Improved High Efficiency Inverter With H6 Type Configuration to Eliminate CMLC for PV System

S. Shobana \(^1\), J. Padma Priya \(^2\)

\(^1\) PG Student, \(^2\) Asst professor, Department of Electrical Engineering
Sri Lakshmi Ammal Engineering College, Anna University, Chennai, India,
**shobi.srs46@gmail.com**

Abstract—To eliminate the common-mode leakage current in the transformerless photovoltaic system, an improved high efficiency inverter H6 type configuration with Z-source is presented. The Z-source network can perform boost as well as sustained shoot through operation. Also, the improved transformerless inverter can sustain the same low input voltage as the full-bridge inverter and guarantee to completely meet the condition of eliminating common-mode leakage current. The sinusoidal pulse width modulation (SPWM) control strategy has applied to implement the presented inverter. Moreover, the higher frequency and lower current ripples are obtained by adopting the double-frequency SPWM, and thus the total harmonic distortion of the PV system is reduced greatly.

I. INTRODUCTION

Photovoltaic (PV) is a method of generating electrical power by converting solar radiation into direct current electricity using semiconductors that exhibit the photovoltaic effect. Photovoltaic power generation employs solar panels composed of a number of solar cells containing a photovoltaic material.

Most of the commercial PV inverters employ either line-frequency or high-frequency isolation transformers. However, line frequency transformers are large and heavy, making the whole system bulky and hard to install. Topologies with high-frequency transformers commonly include several power stages, which increases the system complexity and reduces the system efficiency. Consequently, the transformerless configuration for PV systems is developed to offer the advantages of high efficiency, high power density and low cost. Unfortunately, there are some safety issues because a galvanic connection between the grid and the PV array exists in the transformerless systems. A common-mode leakage current flows through the parasitic capacitor between the PV array and the ground once a variable common-mode voltage is generated in transformerless grid-connected inverters.

The common-mode leakage current increases the system losses, reduces the grid-connected current quality. The H6 inverter has advantages are high efficiency over a wide load range by using MOSFETs for all active switches since their intrinsic body diodes are naturally inactive and low ground leakage current because the voltage applied to the parasitic ground-loop capacitance contains only low frequency components.

The unique feature of the Z-source inverter is that the output ac voltage can be any value between zero and infinity regardless of the fuel-cell voltage. That is, the Z-source inverter is a buck–boost inverter that has a wide range of obtainable voltage.

II. Z- SOURCE NETWORK

![Z-Source network](image)
It employs a unique impedance network (or circuit) to couple the converter main circuit to the power source, load or another converter for providing unique features that cannot be observed in the traditional V and I-source converters where a capacitor and inductor are used, respectively. The Z-source converter overcomes the above-mentioned conceptual and theoretical barriers and limitations of the traditional V-source converter and I-source converter, a two-port network that consists of a split-inductor and capacitors and connected in X shape is employed to provide an impedance source (Z-source) coupling the converter (or inverter) to the dc source, load or another converter. The dc source/or load can be either a voltage or a current source/or load. Therefore, the dc source can be a battery, diode, rectifier, thyristor, converter, fuel cell, an inductor, a capacitor or a combination of those. Switches used in the converter can be a combination of switching devices and diodes such as the antiparallel combination, the series combination two, three-phase Z-source inverter configurations. The inductance and can be provided through a split inductor or two separate inductors.

The traditional three-phase V-source inverter has six active vectors when the dc voltage is impressed across the load and two zero vectors when the load terminals are shorted through either the lower or upper three devices, respectively. When, the inverter bridge is in the shoot-through zero state. Equivalent circuit of the Z-source inverter viewed from the dc link when the inverter bridge is in one of the eight non shoot-through switching states(or vector) when the load terminals are shorted through both the upper and lower devices of any one phase leg, any two phase legs or all three phase legs. This shoot-through zero state (or vector) is forbidden in the traditional V-source inverter, because it would cause a shoot-through. Third zero state (vector) the shoot-through zero state (or vector), which can be generated by seven different ways: shoot-through via any one phase leg, combinations of any two phase legs and all three phase legs. The Z-source network makes the shoot-through zero state possible. This shoot-through zero state provides the unique buck-boost feature to the inverter. Fig.1 shows the circuit of a z-source network.

A two-port network that consists of a split-inductor and capacitors connected in X shape is employed to provide an impedance source (Z-source) coupling the converter (or inverter) to the dc source, load or another converter. The dc source/or load can be either a voltage or a current source/or load. Therefore, the dc source can be a battery, diode rectifier, thyristor converter, fuel cell, an inductor, a capacitor or a combination of those. The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to-ac and dc-to-dc power conversion.

III. HIGH EFFICIENT INVERTER (H5, H6)

A solid-state H-bridge is typically constructed using opposite polarity devices, such as PNP BJTs or P-channel MOSFETs connected to the high voltage bus and NPN BJTs or N-channel MOSFETs connected to the low voltage bus. A common variation of this circuit uses just the two transistors on one side of the load, similar to a class AB amplifier. Such a configuration is called a “half bridge”. The half bridge is used in some switched-mode power supplies that use synchronous rectifiers and in switching amplifiers. The half-H bridge type is commonly abbreviated to “Half-H” to distinguish it from full (“Full-H”) H bridges. Another common variation, adding a third ‘leg’ to the bridge, creates a three-phase inverter. Fig.2 shows the circuit diagram of the conventional inverter with H5-type configuration.
A further variation is the half-controlled bridge, where one of the high and low-side switching devices (on opposite sides of the bridge) are replaced with diodes. This eliminates the shoot-through failure mode and is commonly used to drive variable/switched reluctance machines and actuators where bi-directional current flow is not required.

A "double pole double throw" relay can generally achieve the same electrical functionality as an H bridge (considering the usual function of the device). An H-bridge would be preferable to the relay where a smaller physical size, high speed switching or low driving voltage is needed or where the wearing out of mechanical parts is undesirable.

IV. PROPOSED H6 TYPE INVERTER

The H6 inverter, Fig.3 shows the circuit diagram of the proposed inverter with H6-type configuration, which is composed of six power MOSFETs (S1-S6), two freewheeling diodes (D1 and D2) and two split inductors (L1 and L2) as a low-pass filter. It has advantages are, No need for limited lifetime electrolytic capacitors for a split dc link similar to that of the half-bridge family of inverters with two or three levels. Smaller output inductance as compared to that of the common full-bridge inverter with bipolar PWM switching. Low output ac current distortion because there is no need to have dead time for the proposed circuit since the same phase-leg. A common use of the H-bridge is an inverter. The arrangement is sometimes known as a single-phase bridge inverter. The H-Bridge with a DC supply will generate a square wave voltage waveform across the load. For a purely inductive load, the current waveform would be a triangle wave, with its peak depending on the inductance, switching frequency and input voltage.

IV. CONDITION OF ELIMINATING CMLC

Without an isolated transformer in the PV grid-connected power systems, there is a galvanic connection between the grid and the PV array, which may form a common-mode resonant circuit and induce the common-mode leakage current. The simplified equivalent model of the common-mode resonant circuit has been derived and as shown in fig 4. Where, \( C_{PV} \) is the parasitic capacitor, \( L_A \) and \( L_B \) are the filter inductors, \( i_{cm} \) is the common-mode leakage current and an equivalent common-mode voltage \( u_{ecm} \) is defined by,

\[
\frac{u_{ecm} = u_{cm} + u_{dm}}{2} = \frac{L_B - L_A}{L_A + L_B}
\]

(1)

Fig. 4 Simplified equivalent model of common-mode resonant circuit.
Where, $u_{cm}$ is the common-mode voltage, $u_{dmm}$ is the differential mode voltage, $u_{AN}$ and $u_{BN}$ are the output voltages of the inverter relative to the negative terminal N of the dc bus as the common reference,

$$u_{cm} = \frac{u_{AN} + u_{BN}}{2}$$

$$u_{dmm} = \frac{u_{AB} = u_{AN} - u_{BN}}{2}$$

$$u_{ecm} = \frac{u_{cm} + u_{dmm}}{2}$$

It is clear that the common-mode leakage current $i_{cm}$ is excited by the defined equivalent common-mode voltage $u_{ecm}$. Therefore, the condition of eliminating common-mode leakage current is drawn that the equivalent common-mode voltage $u_{ecm}$ must be kept a constant as follows:

$$u_{ecm} = \frac{u_{AN} + u_{BN} + u_{AN} - u_{BN}}{2} = \text{constant}$$

In the half-bridge inverter family, including NPC inverter, Karschny inverter, and the inverter with two paralleled buck converters, one of the filter inductors $LA$ and $LB$ is commonly zero. Therefore, the condition of eliminating common-mode leakage current is accordingly met that,

$$u_{ecm} = \frac{u_{AN} + u_{BN}}{2} = \text{constant}$$

Similarly, in the full-bridge inverter family including H5 inverter, HERIC inverter, the full-bridge inverter with dc bypass, and the high-efficiency inverter with H6-type configuration, the filter inductors $LA$ and $LB$ are commonly selected with the same value. As a result, the condition of eliminating common-mode leakage current is met that,

$$u_{ecm} = \frac{u_{AN} + u_{BN}}{2} = \text{constant}$$

V. PROPOSED INVERTER TOPOLOGY AND OPERATION ANALYSIS

The PWM scheme for the proposed inverter as shown in Fig 6. The top device in one leg and the bottom device in the other leg are switched simultaneously in the PWM cycle and the middle device operates as a polarity selection switch in the grid cycle as shown if the sinusoidal control voltage $v_{control}$, which is synchronized with grid voltage, is higher than the triangular carrier voltage $v_{carrier}$, the gating voltage G1 and G6 are active; otherwise, G1 and G6 are inactive. And if $v_{control}$ is higher than zero, the gating voltage G4 is active; otherwise, G4 is inactive. Similarly, the comparison of $-v_{control}$ with $v_{carrier}$ or zero results in the logical signals to control G2, G5 and G3 respectively. Fig a shows the four topological stages in one grid cycle for the proposed inverter. Note that the point N is the dc link negative terminal and the point E is the grid negative terminal.
The four operation modes are briefly described as follows. During the grid positive half cycle, switch S4 remains on, whereas S1, S6 and D1 commutate at the PWM switching frequency. When S1, S6 and S4 are on and the other switches and diodes are off, the inductor current is charging, as shown in Fig.a. Under the condition that the inductance values of L1 and L2 are identical, the inductor voltage can be found as,

\[ V_{L1} = V_{L2} = 0.5 (V_{DC} - V_G) \] (8)

And the grid voltage \( V_G \) is calculated by

\[ V_G = V_{DC} \cdot M \cdot \sin (\omega t) \] (9)

Where, \( V_{DC} \) is the dc link voltage; \( M \) is the modulation index and \( \omega t \), is the angular frequency of the grid.

From (8) and (2), the ground potential \( V_{EN1} \) in the charging interval during positive grid half cycle can be expressed,

\[ V_{EN1} = 0.5 \cdot V_{DC} \cdot [1 - M \cdot \sin (\omega t)] \] (10)

In the freewheeling interval during the positive grid half cycle shown in Fig.b. The S1 and S6 simultaneously turn off and S4, D1 are on. The voltages of the inductor L1 and L2 are given as

\[ V_{L1} = V_{L2} = -0.5 \cdot V_G \] (11)

Under the condition that the S1 and S6 share the dc link voltage when they are simultaneously turned off, the voltage stress of the S6 can be found as,

\[ V_{S6} = 0.5 \cdot V_{DC} \] (12)

From (9), (11) and (12), the ground potential \( V_{EN2} \) in the freewheeling interval during positive grid half cycle can be expressed as,

\[ V_{EN2} = 0.5 \cdot V_{DC} \cdot [1 - M \cdot \sin (\omega t)] \] (13)
Based on the fact that (13) is identical to (10), the PWM switching frequency voltage of the ground potential is avoided. The operation modes similarly change during the grid negative half cycle.

From Fig. 5 it can be seen that the body diodes of the MOSFETs are naturally inactive and the high-frequency voltage of the ground potential is avoided during the whole grid cycle. As a result, MOSFETs can be employed as all the active switches and high ground leakage current can be avoided.

The output inductance can be calculated based on the design criterion that the maximum magnitude of the peak-to-peak current ripple is less than (10~20) % of the rated output current $I_{\text{rated}}$. The peak-to-peak inductor current ripple can be derived as,

$$\Delta I_{\text{pk}} = \left( V_{\text{DC}} - V_G \right) \cdot D \cdot T_s / (L_1 + L_2)$$

And the duty cycle $D$ in the proposed inverter is calculated by,

$$D = M \cdot \sin(\alpha \omega) \quad (14)$$

From (14), (13) the peak-to-peak ripple of the inductor current can be derived as

$$\Delta i_{\text{pk}} = 0.25 \cdot V_{\text{DC}} \cdot T_s \left[ 1 - \left( 1 - 2M \sin(\alpha \omega) \right)^2 \right] / (L_1 + L_2)$$

Where, $T_s$ is the PWM switching period. When,

$$1 - 2M \sin(\alpha \omega) = 0$$

Fig. 6 PWM scheme for the proposed inverter: (a) signals in time domain;

The maximum peak-to-peak ripple of the inductor current in the whole grid cycle is calculated by,

$$\Delta i_{\text{pk, max}} = 0.25 \cdot V_{\text{DC}} \cdot T_s \leq (10 \sim 20) \% I_{\text{rated}} \quad (16)$$

In the proposed inverter, the output inductance then can be calculated as

$$(L_1 + L_2) \geq \frac{0.25 \cdot V_{\text{DC}} \cdot T_s}{(10 \sim 20) \% I_{\text{rated}}} \quad (17)$$

$$L_{\text{out}} \geq \frac{0.5 \cdot V_{\text{DC}} \cdot T_s}{(10 \sim 20) \% I_{\text{rated}}} \quad (18)$$

Thus, the output inductance in the proposed inverter is half that of the conventional full-bridge inverter using bipolar PWM scheme.
VI. CONTROL STRATEGIES

A. Unipolar SPWM strategy

In the positive half cycle, $S_1$ and $S_6$ are always ON. $S_4$ and $S_5$ commutate at the switching frequency with the same commutation orders. $S_2$ and $S_3$ respectively, commutate complementarily to $S_1$ and $S_4$. Accordingly, Mode 1 and Mode 2 continuously rotate to generate $+U_{dc}$ and zero states and modulate the output voltage. Likewise, in the negative half cycle, Mode 3 and Mode 4 continuously rotate to generate $-U_{dc}$ and zero states as a result of the symmetrical modulation.

![Ideal waveforms of the improved inverter with unipolar SPWM](image1)

**Mode 1:**
When $S_4$ and $S_5$ are ON, $u_{AB} = +U_{dc}$ and the inductor current increases through the switches $S_5$, $S_1$, $S_4$ and $S_6$. The common-mode voltage is,

$$ucm = \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}(U_{dc} + 0) = \frac{U_{dc}}{2} \quad (19)$$

**Mode 2:**
When $S_4$ and $S_5$ are turned OFF, the voltage $u_{AN}$ falls and $u_{BN}$ rises until their values are equal and the anti-parallel diode of $S_3$ conducts. Therefore, $u_{AB} = 0V$ and the inductor current decreases through the switch $S_1$ and the anti-parallel diode of $S_3$. The common-mode voltage changes into,

$$ucm = \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}(U_{dc}/2 + U_{dc}/2) = \frac{U_{dc}}{2} \quad (20)$$

**Mode 3:**
When $S_3$ and $S_6$ are ON, $u_{AB} = -U_{dc}$ and the inductor current increases reversely through the switches $S_5$, $S_3$, $S_2$ and $S_6$. The common-mode voltage becomes,

$$ucm = \frac{1}{2}(u_{AN} + u_{BN}) = \frac{1}{2}(0 + U_{dc}) = \frac{U_{dc}}{2} \quad (21)$$

**Mode 4:**
When $S_3$ and $S_6$ are turned OFF, the voltage $u_{AN}$ rises and $u_{BN}$ falls until their values are equal and the anti-parallel diode of $S_4$ conducts. Similar as to Mode 2, $u_{AB} = 0V$ and the inductor current decreases through the switch $S_2$ and the anti-parallel diode of $S_4$. The common-mode voltage $ucm$ also keeps $U_{dc}/2$.

From (19) to (21), the common-mode voltage can remain a constant $U_{dc}/2$ during the four commutation modes in the improved inverter with unipolar SPWM. The switching voltages of all commutating switches are half of the input voltage $U_{dc}/2$, and thus, the switching losses are reduced compared with the full bridge inverter.

Furthermore, in a grid period, the energies of the switching losses are distributed averagely to the four switches $S_3$, $S_4$, $S_5$ and $S_6$ with high-frequency commutations and it benefits the thermal design of printed circuit board and the life of the switching components compared with H6 inverter.

B. Double-frequency SPWM strategy

The improved inverter can also operate with the double frequency SPWM strategy to achieve a lower ripple and higher frequency of the output current. In this situation, both phase legs of the inverter are, respectively, modulated with 180° opposed reference waveforms and the switches $S_1$–$S_4$ all acting at the switching frequency. Two additional switches $S_5$ and $S_6$ also
commutate at the switching frequency cooperating with the commutation orders of two phase legs. Accordingly, there are six operation modes to continuously rotate with double frequency and generate \( +U_{dc} \) and zero states or \( -U_{dc} \) and zero states, as shown in modes of operation shows the ideal waveforms of the improved inverter with double-frequency SPWM.

In the positive half cycle, \( S_6 \) and \( S_1 \) have the same commutation orders and \( S_5 \) and \( S_4 \) have the same orders. \( S_2 \) and \( S_3 \) respectively, commutate complementarily to \( S_1 \) and \( S_4 \). Accordingly, Mode 1, Mode 2 and Mode 5 continuously rotate to generate \( +U_{dc} \) and zero states and modulate the output voltage with double frequency. In the negative half cycle, Mode 3, Mode 4 and Mode 6 continuously rotate to generate \( -U_{dc} \) and zero states with double frequency due to the completely symmetrical modulation.

Mode 5:
When \( S_1 \) and \( S_6 \) are turned OFF, the voltage \( u_{AN} \) falls and \( u_{BN} \) rises until their values are equal and the anti-parallel diode of \( S_2 \) conducts. Therefore, \( u_{AB} = 0V \) and the inductor current decreases through the switch \( S_4 \) and the antiparallel diode of \( S_2 \). The common-mode voltage \( u_{cm} \) keeps a constant \( U_{dc}/2 \).

Mode 6:
Similarly, when \( S_2 \) and \( S_5 \) are turned OFF, the voltage \( u_{AN} \) rises and \( u_{BN} \) falls until their values are equal and the antiparallel diode of \( S_1 \) conducts. Therefore, \( u_{AB} = 0V \) and the inductor current decreases through the switch \( S_3 \) and the antiparallel diode of \( S_1 \). The common-mode voltage \( u_{cm} \) still is a constant \( U_{dc}/2 \). Under the double-frequency SPWM strategy, the common mode voltage can keep a constant \( U_{dc}/2 \) in the whole switching process of six operation modes. Furthermore, the higher frequency and lower current ripples are achieved and thus, the higher quality and lower THD of the grid-connected current are obtained or a smaller filter inductor can be employed and the copper losses and core losses are reduced.

The practical waveforms of the improved inverter when considering the phase shift, where \( u_{AB} \) is the fundamental component of the output voltage. In Region I and Region II, the detailed operation principle and modes of the unipolar SPWM and double-frequency SPWM have been analyzed earlier, under the condition that the output voltage and current are in the same direction. In Region III, the output current is positive. Meanwhile, the output voltage is negative and modulated according to the operation principle in the positive half cycle.

Therefore, if the unipolar SPWM strategy is adopted, accordingly Mode 7 and Mode 5 continuously rotate to generate \( -U_{dc} \) and zero states. If the double-frequency SPWM strategy is used Mode 7, Mode 2 and Mode 5 continuously rotate to generate \( -U_{dc} \) and zero states with double frequency.

Symmetrically in Region IV, the output current becomes negative and the output voltage is modulated according to the operation principle in the positive half cycle. Hereby, Mode 8 and Mode 6 continuously rotate to generate \( +U_{dc} \) and zero states when the unipolar SPWM strategy is used. Mode 8, Mode 4 and Mode 6 continuously rotate to generate \( +U_{dc} \) and zero states with double frequency when, the double-frequency SPWM is adopted.

Mode 7:
Although the switches \( S_2, S_5, S_3 \) and \( S_6 \) are ON and \( S_1, S_4 \) are OFF, the positive inductor current only free wheels through the anti-parallel diodes \( S_3, S_5, S_6 \) and \( S_2 \) decreases rapidly for enduring the reverse voltage. The common-mode voltage \( u_{cm} \) keeps \( U_{dc}/2 \).
Mode 8:
Similarly, the negative inductor current only free wheels through the anti-parallel diodes of $S1$, $S5$, $S6$ and $S4$ decreases rapidly for enduring the reverse voltage. The common-mode voltage $u_{cm}$ still keeps $U_{dc}/2$ referred.

VII. SIMULATION RESULT

An improved grid-connected inverter topology for transformerless PV systems is presented, which can sustain the same low input voltage as the full-bridge inverter and guarantee not to generate the common-mode leakage current. Furthermore, both the unipolar SPWM and the double-frequency SPWM with three-level output can be applied in the presented inverter. The high efficiency and convenient thermal design are achieved by adopting the unipolar SPWM. Moreover, the higher equivalent frequency and lower current ripples are obtained by using the double-frequency SPWM. Therefore, a smaller filter inductor can be employed and the harmonic contents and total harmonic distortion (THD) of the output current are reduced greatly and the grid-connected power quality is improved accordingly.

The condition of eliminating common-mode leakage current is analyzed in Section II. The improved inverter topology and correlative operation modes under two SPWM control strategies are introduced in Section III. The influence of the power switches’ junction capacitances is illustrated in Section IV. The simulated and experimental results are shown in Section V to explore the performance of the presented inverter. Section VI summarizes the conclusions drawn from the investigation.

OUTPUT VOLTAGES
The below waveform shows the output voltage of the normal waveform are shown in fig. 11 and 12.
The experimental waveform which is similar to the simulation, but the resonant amplitude is slightly damped due to the internal resistance of the practical inverter prototype.

Therefore, to accord with the value principle of the junction capacitors under the unipolar SPWM, two additional capacitors with the values of 29 pF are respectively, paralleled to $S3$ and $S4$. It is clear that the grid-connected current is highly sinusoidal synchronized with the grid voltage by achieving the three-level output. Similarly, to accord with the value principle of the junction capacitors under the double-frequency SPWM, four additional capacitors are respectively paralleled to $S1$–$S4$ whose values are much larger than the junction capacitances of $S5$ and $S6$ . However, considering the increased switching losses induced by the paralleled capacitors, the value of the paralleled capacitor is decided as 470 pF as a tradeoff. Therefore, $u_{{AN}} = u_{{BN}} = 0.514U_{{dc}}$ is obtained at the end point of the transient process from Mode 1 to Mode 2 and thus, $u_{{cm}}$ is maintained at $U_{{dc}}/2$ approximately.

VIII. CONCLUSION

This paper presented an improved grid-connected inverter topology for transformerless PV systems. The unipolar SPWM and double-frequency SPWM control strategies are both implemented with three-level output in the presented inverter, which can guarantee not to generate the common-mode leakage current because the condition of eliminating common-mode leakage current is met completely. Furthermore, the switching voltages of all commutating switches are half of the input dc voltage and the switching losses are reduced greatly. Moreover, by adopting the double-frequency SPWM, the higher frequency and lower current ripples are achieved. Consequently, the higher quality and lower THD of the grid-connected current are obtained or the smaller filter inductors are employed and the copper losses and core losses are reduced accordingly. Finally, a 1-kW prototype was built and the validity and applicability of the improved inverter were confirmed by the simulated and experimental results.

References