An Innovative VLSI Algorithm Design Technique To Reduce Leakage Current In CMOS VLSI Circuits

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Abstract-In this paper we give the introduction to leakage current and methods to minimize the leakage current. Further we also present the evaluation of various methods to minimize the leakage current in CMOS VLSI circuits with the proposed ideas. Process Modification method is one of the method to minimize the leakage current, the other method is the Circuit level modifications, and in this paper these modification techniques are described effectively.

Keywords- CMOSVLSI, Leakage Current, Pipelining, Power dissipation, Voltage Scaling

I. INTRODUCTION

The importance of leakage current is stated in terms of major power dissipation which is implied by its dynamic power. It is given by the equation $P_D = C_0 * V_{DD}^2 * f$, Voltage scaling has resulted in reduction of dynamic power. But increased static power dissipation due to reduced $V_{TH}$. Leakage power is larger percentage of total chip power in watts. The devices such as mobile phone, calculator have low-on time, large stand by period, which results in almost equal static and dynamic power dissipation. Also there is poor refresh times in D-RAM’S.

II. SOURCES OF LEAKAGE CURRENT

There are three main sources of leakage current, they are source/drain junction currents, Subthreshold leakage, gate tunnelling currents. The source/drain junction current is given by the generalised equation $I_{DS} = K \cdot \exp(\frac{-V_{DS}}{\eta V_T}) \cdot \exp(\frac{V_{GS} - V_{TH}}{n V_T}) \cdot \exp(\frac{1.8}{\eta V_{DS}})$, where $K = \mu_o C_{ox} W_{eff} L_{off} / L_{eff}$, $\eta$ is process dependent parameter.

$V_T$ is voltage equivalent of temperature and $\eta$ is drain induced barrier lowering coefficient.

The gate tunnelling current is given by the equation

$I_{GT} = \exp(-B(1-V_{OX}/\phi_{OX})^1.5) / (V_{OX} / T_{OX})^2 \cdot \exp(V_{OX}/T_{OX})^2 \cdot \exp(-T_{OX}/T_{OX})^2$.

Where $I_{GT}$ is propotional to the $\exp(V_{OX}) 2$, further $I_{GT}$ is propotional to $\exp(\phi_{OX}/T_{OX})^2$.

III. METHODS TO MINIMIZE THE LEAKAGE CURRENT

There are two methods to minimize the leakage current, they are given by process modifications and Circuit level modifications. Process Modification method is one of the method to minimize the leakage current, the other method
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is the Circuit level modifications. In process modification the threshold voltage is increased during the fabrication process, further during process modification the gate oxide thickness and materials are changed.

$$V_{TH}=V_{fb}+2q\phi_b+\sqrt{(2e_o q N_A (2q\phi_b+|V_{SB}|)/C_{OX}}$$

where, $V_{fb}$ is flatband voltage, $\phi_b$ is the bulk potential $kT/q\ln(N_A/N_i)$, $C_{OX}$ is the oxide capacitance given by $\frac{\varepsilon_{ox}}{t_{ox}}$. As the gate oxide thickness and materials are changed then $I_{GT}$ is proportional to $\exp(-T_{OX}/T_{OX})^2$

Further greater is the $T_{OX}$ then lesser is the gate tunneling. Reduced subthreshold leakage due to increased $V_{TH}$. Further the gate capacitance is reduced and hence dynamic power is reduced.

To maintain constant $C_{OX}$ we need material with higher $\varepsilon_{ox}$. For example Oxinitrides have $k\approx 4.1-4.2$ as compared to $SiO_2(k=3.9)$. Further in the evaluation of gate oxide no additional hardware control is required. There is increase in $T_{OX}$ lowers the speed. Process modification is difficult in some cases. MTCMOS increases delay, but no additional hardware is required. Further there is the need of an algorithm to search non-critical paths. And noise immunity problems also arises.

IV. INNOVATIVE APPROACH FOR EFFICIENT IMPLEMENTATION OF PIPELINING

Pipelining is a popular method in computer architecture to increase speed of execution. An instruction is subdivided into various independent parts. Each part is executed separately by dedicated units. Various stages of typical pipelined structure is given by

1. Instruction fetch
2. Decode & Register fetch
3. Execute
4. Data fetch (memory)
5. Write back to memory

![Figure 1 Pipelining Concept](image)

For proper operation all the parts must be synchronized accurately. But all the parts definitely differ in the delay introduced. The unit offering maximum delay is considered as the critical path. The System is operated at this speed, with registers storing intermediate values. The innovative approach that we suggest is to intentionally increase the delay of the non-critical stages (decoder and ALU), within the critical time (<50 $\mu$s); by MTCMOS/Gate oxide etc. Greater the Leakage current is reduced and the functionality is not affected.
Further to vary gate thickness and/or channel length at random is difficult. Therefore we propose to divide the whole chip into several blocks. The transistor dimensions are constant within a block but vary from one to another as shown in the layout below.

![Figure 2 Layout to incorporate different stages of pipeline](image)

The drawback here is area overhead due to increased channel length. Further the more cost is involved in process modifications. The solution here is the area overhead can be minimized if we go for varying the oxide thickness instead of channel length. Alternatively we can go for insertion of passive resistance lines using Meander patterns, where area overhead is tolerable but process modification is not tolerable.

![Figure 3 Insertion of passive resistance lines.](image)

Power-delay product is constant for a given technology and it is far greater than dynamic power which also reduces for increased delay. If the delays of all the stages are matched then more area and power can be saved. This is achieved by removing the intermediate memory registers, provided that there are no pipeline hazards.

V. CIRCUIT LEVEL MODIFICATIONS

The circuit level modifications involves five steps

1. Gating power supply
2. Body bias control
3. PMOS based design
4. NOR structures
5. Input Vector Control

In Gating power supply shut down the power supply to the units that are idle. This requires special power supply gating transistors with high $V_{TH}$ controlled by ‘sleep’ signal.

In Body bias control the increase in threshold voltage ($V_{TH}$) reduces subthreshold leakage

$$V_{TH} = V_{fb} + 2\phi_b + \sqrt{2}\phi_b qN_A(2\phi_b + |V_{SB}|) / C_{OX}$$

More is the $V_{SB}$ then more will be the value of $V_{TH}$

In PMOS and NMOS structures Gate tunneling is less in case of holes due to lesser mobility which implies that PMOS better than NMOS for ‘sleep’ transistor. Also gate tunneling is observed to be less in NOR structures.
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In Input Vector Control (IVC) the subthreshold current depends on the applied input vector that is both values and position. Using a simple logic circuit we can determine the minimum leakage vector (MLV) for the given circuit.

![Figure 4 Input Vector Control Pattern](image)

We consider the leakage current for NAND3 which is as follows,

<table>
<thead>
<tr>
<th>State</th>
<th>I(leak) in pico-amps</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>3.21</td>
</tr>
<tr>
<td>001</td>
<td>4.62</td>
</tr>
<tr>
<td>010</td>
<td>4.67</td>
</tr>
<tr>
<td>011</td>
<td>31.30</td>
</tr>
<tr>
<td>100</td>
<td>6.47</td>
</tr>
<tr>
<td>101</td>
<td>32.10</td>
</tr>
<tr>
<td>110</td>
<td>36.70</td>
</tr>
<tr>
<td>111</td>
<td>32.30</td>
</tr>
</tbody>
</table>

Table 1 Leakage Current for NAND3

During standby mode the gates are forced with the stored MLV. This can be done by using built-in scan chains which avoid the extra hardware. The benefits are more only if the standby period is large.

We further describe the Input Vector Control using the scan chain as given in figure 5. This requires additional hardware and can be implemented during the run time.
In PMOS & NOR Structures the constraint is on the designer, further the large area is consumed both by PMOS and strictly NOR based logic. Further evaluation of power supply gating requires High $V_{TH}$ transistors with low on-state resistance. The gating supply for a large circuit is difficult.

In the evaluation of Interrupt Vector Control (IVC) there is no additional hardware for applying the minimum leakage vector (MLV), if scan chain is used, hardwiring the minimum leakage vector (MLV) is easy. But ‘n’ clocks needed to apply minimum leakage vector (MLV) which is useful only for ‘longer’ standby period. There is extra hardware will be required for storing minimum leakage vector (MLV).

The scope for improving the Input Vector Control (IVC) lies in applying the minimum leakage vector in a single clock, this is achieved by hardwire connection for all or group of inputs, further the latches are disabled by the ‘sleep’ signal.

In the calculations for a 1000-bit minimum leakage vector (MLV), the Scan chain method needs 1000 clocks + 1000-bit shift register (6000 transistors) and modified Latch method needs 1000 transistors.
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The method as shown in figure 6 needs 20 buffers ~100 transistors (Fanout=50). 10% of hardware overhead compared to previous method implies lower dynamic power loss (switching during application of MLV). Excess leakage due to control hardware is reduced.

\[
\text{Minimum idle time reduced}
\]
\[
t_{\text{idle}} > (E_t + t_{\text{tot}} P_{\text{exleak}})/(P_{\text{leak}} - P_{\text{exleak}} - P_{\text{min}}) \tag{5}
\]

Where,

- \(P_{\text{leak}}\) - leakage without IVC,
- \(P_{\text{min}}\) - leakage with IVC

If \(E_t\) is transition energy \(E_{\text{tr}}\) for previous method and \(P_1\) is excess leakage due to control hardware. For a method as shown in figure 6

\(E_{\text{tr}} = 10\% E_{\text{tr}} \) and \(P_{\text{exleak}} \approx 10\% P_1\)

The problems associated with this are the fanout problems for power supply to input latches and for input buffers. The solution for this above problem is to increase the control transistors and add more buffers.

Further Number of Buffers = Number of Inputs/Fanout

Next we describe the simple flow chart to add more buffers as shown in figure 7.

Here the power supply (sleep) transistors need to have very low On-state resistance, or we need more such transistors

No. of sleep transistors = length(MLV)*I_L*R_{on}/V_{DD}

r = voltage regulation, I_L = latch current,

R_{on} = on-state resistance of sleep transistor

<table>
<thead>
<tr>
<th>Method/Parameter</th>
<th>No. of additional Transistors</th>
<th>No. Of Clocks</th>
<th>Dynamic Power</th>
<th>Excess Power Source</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scan Chain</td>
<td>6000 (1000 bit shift registers)</td>
<td>1000</td>
<td>1000*1000 *( \phi_2 / 2)</td>
<td>SR, Scan Chain</td>
<td>More Clocks, State recovery with extra Hardware</td>
</tr>
<tr>
<td>Modified Latch</td>
<td>1000</td>
<td>1</td>
<td>1000*Pt</td>
<td>1000 transistors</td>
<td>Little extra hardware 1 clock</td>
</tr>
<tr>
<td>As seen in Figure 6</td>
<td>~100</td>
<td>1</td>
<td>20*( \phi_2 = 1 ) 60*Pt</td>
<td>~100 transistors</td>
<td>Very less extra hardware 1 clock</td>
</tr>
</tbody>
</table>

Table 2 Comparision of IVC Methods
VI. FUTURE SCOPE

Here the future scope of improvement involves the rigorous study of power-delay relations for CMOS circuits, further study the effect of delayed stages on performance of pipeline on actual hardware. Study of fanout capabilities of CMOS circuits and State recovery in IVC. The Placement & Routing Algorithms for efficient pipelined structures can be designed and implemented.

VII. CONCLUSION

The importance of the leakage current is stated in terms of major power dissipation which is implied by its dynamic power. The sources of leakage and methods to minimize the leakage current and their comparison is discussed in detail in terms of process modifications and circuit level modifications. Proposed methods involve efficient pipeline structure and improved IVC.

VIII. REFERENCES