Design Issues with a Synchronous Buck Converter for VRM

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Abstract-
Switched Mode Power Supplies (SMPS) are very important components in present day electronics. The present day competition in the power supply in meeting the requirements of the future microprocessors has led to the incorporation of one or the other salient features in the design of the power supply. There is a tremendous improvement in the performance of the CPUs right from 8086 to present day i7 processor. As there is an increase in the speed of operation of the processor and the storage capacity, there is an increase in the power consumption too. Thus, there is a necessity of dedicated DC-DC converter at the close proximity of the processor. A synchronous buck converter is found to be suitable to meet this demand. Efficiency is often the primary design goal when using a dc/dc converter. Many design requirements involve converting the battery voltage to a low supply voltage. Design simplicity, low component count, and lower cost make buck converters popular solutions where low input voltages are available for the converter and where isolation is not a requirement. This paper presents design parameters for a Synchronous Buck Converter used as a voltage regulator module for microprocessors.

Key words – synchronous buck converter, efficiency, dc-dc converter, input voltage, switching frequency

I. Introduction.
A buck converter is a non-isolated dc-dc converter which produces a lower average output voltage than the dc input voltage. It is a switching mode regulator since it makes use of the switching action of a semiconductor device such as power BJTs or MOSFETs to manipulate the dc output voltage. This converter is widely used in power management, microprocessor voltage regulator modules (VRM’s) and dc motor speed control applications

The term non-isolated refers to the presence of a common voltage reference node between the input and output of the converter [3].

1.1 Operation of the Buck Converter
The topology of the buck converter is shown in figure below. The switch shown may implemented by using either a power BJT or MOSFET.

The inductor and capacitor form a low pass filter which helps to diminish the output voltage fluctuations. The waveform of the input \( v_i \) to the low pass filter is as shown in figure 1.1
During the interval when the switch is on, the diode becomes reversed biased and the input provides energy to the load as well as to the inductor. During the interval when the switch is off, the inductor current flows through the diode, transferring some of its stored energy to the load [1].

2 Steady State Analysis

The steady state analysis of buck converter is elaborately discussed in Ref. [1], [4]. The following properties are satisfied by the buck converter (and dc-dc converters in general) when operating in the steady state [4],

- The inductor current is periodic:
  \[ i_L(t + T) = i_L(t) \] ................. (2.1)

- The average inductor voltage is zero:
  \[ V_L = \frac{1}{T} \int_0^T v_L(\lambda) d\lambda = 0 \] ....... (2.2)

- The average capacitor current is zero:
  \[ i_C = \frac{1}{T} \int_0^T i_C(\lambda) d\lambda = 0 \] ..... (2.3)

The power supplied by the source is same as the power delivered to the load. For non-ideal components the source also supplies the losses.

We carry out the steady state analysis of the buck converter under following assumptions:

- The inductor current is always positive (continuous conduction mode)
- The filter capacitor is very large so that the instantaneous output voltage is nearly constant.
- The switching period is \( T_s \); the switch is closed for time \( t_{on} \) and open for time \( t_{off} \).
- The components of the buck converter are ideal.

2.1 Derivation of expression for duty ratio

Waveforms for the continuous conduction mode of operation are shown in figure 2.1. During \( t_{on} \), the switch conducts the inductor current and the diode becomes reversed biased, which results in positive a voltage \( v_L = V_o V_o \) to appear across the inductor. This voltage causes a linear increase in inductor current \( i_L \). During \( t_{off} \), \( i_L \) continues to flow because of the stored inductive energy and a path for it is provided by the diode. The voltage across the inductor is now \( v_L = -V_o \).
Thus, \( V_o = \frac{V_o}{T_o} \) \( t_{on} = V_o (T_o - t_{off}) \) ..........(2.4)

Or, \( \frac{V_o}{V_o} = \frac{t_{on}}{T_o} = D \) (duty ratio) .......... (2.5)

According to steady state requirement, which states that volt – second product of the inductor remains the same during On time and Off time.

### 2.2 Derivation for the value of inductor:

As stated in the earlier subsection, when the switch is closed, voltage across the inductor is,

\[ v_L = V_o - V_o = \frac{dL}{dt} \] .................(2.6)

Rearranging,

\[ \frac{dL}{dt} = \frac{V_o - V_o}{L} \]

\[ \frac{dL}{dt} = \frac{\Delta L}{\Delta t} = \frac{V_o - V_o}{L} \]

Thus,

\[ \Delta L_{(cloned)} = \frac{(V_o - V_o) \Delta t}{L} \] .......... (2.7)

And when the switch is open,

\[ v_L = -V_o = L \frac{dL}{dt} \] .................(2.8)

Again by rearranging,

\[ \frac{dL}{dt} = -\frac{V_o}{L} \]

\[ \frac{dL}{dt} = \frac{\Delta L}{\Delta t} = -\frac{V_o}{L} \]

Therefore,

\[ \Delta L_{(open)} = \frac{-V_o (1-D) \Delta t}{L} \] .......... (2.9)

For steady state operation equation (2.1) must be satisfied, which implies, (2.10)
As the change in inductor current is known from equation (2.11), so the maximum and minimum values of the inductor current are computed as:

\[ I_{\text{max}} = I_L + \frac{\delta I_0}{2} = \frac{V_o}{R} + \frac{1}{2} \frac{V_o}{L} (1 - D) T_2 = V_o \left[ \frac{1}{R} + \frac{(1-D)T_2}{2L f_s} \right] \] \hspace{1cm} (2.13)

And

\[ I_{\text{min}} = I_L - \frac{\delta I_0}{2} = \frac{V_o}{R} - \frac{1}{2} \frac{V_o}{L} (1 - D) T_2 = V_o \left[ \frac{1}{R} - \frac{(1-D)T_2}{2L f_s} \right] \] \hspace{1cm} (2.14)

Where \( f_s = 1/T_s \) is the switching frequency.

The minimum value of inductor to ensure operation in the continuous conduction mode is found by evaluating \( I_{\text{min}} \) to zero, since it is the boundary between continuous and discontinuous modes.

Therefore,

\[ I_{\text{min}} = \frac{V_o}{R} \left[ 1 - \frac{(1-D)T_2}{2L f_s} \right] = 0 \]

Or,

\[ I_{\text{min}} = \frac{(1-D)R}{2f_s} \hspace{1cm} (2.15) \]

2.3 Derivation for value of the capacitor

Although the output capacitor was assumed to be large enough to give a nearly constant instantaneous value of the output voltage, the ripple in the output voltage with a practical value of capacitance can be calculated by considering the waveforms shown in Figure 2.2 for a continuous conduction mode of operation. Assuming that the entire component in \( i_i \) flows through the capacitor and its average component flows through the load resistor, the shaded area in Figure 2.4 represents an additional charge \( \Delta Q \).

\[ \Delta V_o = \frac{\Delta Q}{C} = \frac{1}{2} \frac{(1-D)T_2}{2} \] \hspace{1cm} (2.16)

From figure 2.4, during \( f_s \),

\[ \Delta V_o = \frac{V_o}{8L} \frac{1-D}{T_2} \] \hspace{1cm} (2.17)

Thus,

\[ \Delta V_o = \frac{V_o}{8L} \frac{(1-D)T_2}{T_s} \] \hspace{1cm} (2.18)

Therefore,

\[ \Delta V_o = \frac{V_o}{8L} \frac{(1-D)}{T_s} = \frac{V_o}{2} \frac{(1-D)(f_s)^2}{T_s} \] \hspace{1cm} (2.19)

Where, \( f_s = 1/T_s \), is the switching frequency, and

\[ f_c = \frac{1}{2\pi \sqrt{LC}} \] \hspace{1cm} (2.20)
Equation (2.19) shows that the voltage ripple can be minimized by selecting the corner frequency $f_c$ of the low pass filter at the output such that $f_c << f_s$. Also the ripple is independent of the load output power so long the converter operates in continuous conduction mode [1].

If voltage ripple $\Delta V_o$ and ripple current $\Delta I_o$ are specified, then value of capacitance required can be calculated by from equation (2.16)

### 3: SYNCHRONOUS BUCK CONVERTER

The forward voltage of a diode $V_D$ contributes to a decrease in efficiency. This contribution is especially significant in low-output voltage power supplies, for example, 3.3-V power supplies for microprocessors or power supplies for portable telecommunication equipment. Even with a Schottky diode, which has $V_D$ in the range of 0.4 V, the power loss in the diode can easily exceed 10% of the total power delivered to the load [5].

The synchronous buck converter, also known as synchronous rectifier buck converter (SRBC) has the same basic topology as the conventional buck converter, but the freewheeling diode is replaced by a MOSFET so as to provide a low resistance conduction path. The gate drive pulses to the main and synchronous MOSFETs are complementary with respect to each other and sometimes a dead space or dead time is also provided to prevent a shoot through, i.e. a condition when both MOSFETs are in their ‘on’ state which may short the input source.

The synchronous buck converter topology and its gate drive pulses are shown in Figure 3.1

![Synchronous buck converter topology and its gate signals](image)

**Fig. 3.1 Synchronous buck converter topology and its gate signals**

### Efficiency Improvement

The conduction losses are reduced by using a synchronous MOSFET instead of a diode since MOSFETs have very low on state resistance (usually between 10 to 75 mΩ). As the diode conducts only during the off time, so the equation for power loss in a diode can be given by:

$$P_D = V_D \cdot I_o \cdot (1 - D) \cdot \eta_d$$

Let the input dc voltage be 12 V and output dc voltage be 5 V to give $D = 0.4166$. Consider a Schottky diode with $V_D = 0.4$ V, and output current of the converter as 1 A. Then, $P_D$ equals 233.36 mW. For the synchronous MOSFET switch, power loss in its on state is given by:

$$R_s = I_o^2 \cdot (1 - D) \cdot R_{DS(on)}$$

Considering a value of $R_{DS(on)}$ as 45 mΩ, $P_s$ equals 26.25 mW.

It can be seen that the power loss is very much dependent upon the duty cycle. A synchronous rectifier generally has lower losses than a conventional or Schottky diode, and so its use is quite popular in low voltage DC/DC converters [6].

### Difficulties Involved

Design of the gate drive circuitry becomes complicated as we need to drive two MOSFETs and care has to be taken to prevent any shoot through.

### 4: CONVENTIONAL AND SYNCHRONOUS BUCK CONVERTER DESIGN

#### 4.1 Converter Specifications

For designing a practical converter, we need to take into account the various parasitic effects of the components involved.

A practical buck converter design example is discussed in Ref. [7].

Both the conventional and synchronous buck converters are designed for the following specifications:

- Input Voltage, $V_i = 12$ V
- Output Voltage, $V_o = 5$ V
- Load Current, $I_o = 1$ A (so load resistor $R = 5$ Ω)
- Switching Frequency, $f_s = 200$ kHz
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- Duty Ratio, \( D = 0.4166 \) [from equation (2.5)]
- Peak-Peak ripple current is limited to 30\% of load current, so \( \Delta I = 0.3A \)

### 4.2 Calculation for Inductor
By rearranging equation (2.11), we can find the value of the inductor as,

\[
L = \frac{\Delta V}{(\Delta I \cdot ESR)}
\]  

Solving, we get \( L= 48.6 \) \( \mu \)F

A 47 \( \mu \)F inductor with tolerance of ±20\%, rated current of 2.02 A, saturation current of 3.1 A, and maximum dc resistance of 125m\( \Omega \) from Würth Elektronik is selected. It has two windings of 47 \( \mu \)F each, out of which one is used. Also from equation (2.15), we calculate the minimum value of the inductor to ensure operation in the continuous conduction mode as \( L_{min}= 7.29 \) \( \mu \)F. Since, \( L > L_{min} \), so continuous conduction mode of operation is ensured.

### 4.3 Calculation for Output Capacitor
The voltage ripple across the output capacitor is the sum of ripple voltages due to the “Effective Series resistance “(ESR), the voltage sag due to the load current that must be supplied by the capacitor as the inductor is discharged, and the voltage ripple due to the capacitor’s ESL or “Effect Series Inductance” \[7\]. It is given by:

\[
\Delta V_o = \Delta I \cdot (ESR + \Delta T / C + ESL / \Delta T) \]  

As the ESL specification is usually not specified by the capacitor vendor so the ESL value is assumed to be zero. At very high switching frequencies (>1 MHz), the ESL specification becomes more important.

Simplifying equation (4.2) by assuming ESR = 0:

\[
\Delta V = \Delta I \cdot (ESR + \Delta T / C)
\]

Rearranging, we get

\[
C = (\Delta I \cdot \Delta T) / ((\Delta V - (\Delta I \cdot ESR)))
\]

The acceptable output voltage ripple, \( \Delta V_o \), is defined as 50mV and ESR is selected as 0.03 \( \Omega \). Solving equation (4.3) with \( \Delta V_o =50mV, \Delta I = 0.3 A, ESR = 0.03 \Omega, \) and \( \Delta T = (0.4166 / 200 kHz) = 2.083\mu s \), yields the value of capacitor as \( C=15.24\mu F \).

The term in the denominator of equation (4.3), \( (\Delta V - (\Delta I \cdot ESR)) \) shows that the capacitor’s ESR rating is more important than the capacitance value. If the selected ESR is too large, the voltage due to the ripple current will equal or exceed the target output voltage ripple. We will have a divide by zero issue, indicating that an infinite output capacitance is required. When ESR requirement is met, the capacitor’s capacitance is usually adequate. \[7\].

A capacitor of 1200 \( \mu F, 35V \), with ESR of 0.029 \( \Omega \) is selected as it meets the ESR requirements.

### 4.4 Calculation for Input Capacitor
The worst case ripple current occurs when the duty cycle is 50\% and the worst case ripple current on the input of a buck converter is about one half of the load current. Like the output capacitor, the input capacitor selection is primarily dictated by the ESR requirement needed to meet voltage ripple requirements.

Usually, the input voltage ripple requirement is not as stringent as the output voltage ripple requirement \[7\].

The input ripple current is estimated as,

\[
I_{ripple} = \frac{I_i}{2} = 0.5A
\]

We define acceptable input ripple voltage as 200 mv and select a capacitor ESR value of 0.07 \( \Omega \)

The input capacitance is computed using:

\[
C = \Delta T / ((Vripple / Iripple) - ESR) \]  

The above equation yields the value on the input capacitance as 6.31 \( \mu F \).

A 470 \( \mu F, 25V \) with ESR of 0.067 \( \Omega \) is selected as it meets the ESR requirements.

### 4.5 Calculation of Diode Current
The current flowing through the diode to be used in conventional buck converter topology is estimated as,

\[
I_d = (1 - D) \cdot I_o
\]

We use \( D= 0.4166, I_o = 1A \), we find the value of ID as 0.5834 A.

The maximum diode reverse voltage is 12V.

IN5820, a Schottky rectifier with the rating of 3A, 20V is selected as it meets the requirements.
5: SIMULATION RESULTS

5.1 Description
To verify the design of both the conventional and synchronous buck converters, simulation is carried out in the Matlab/Simulink environment. The values of the components for the simulation are chosen as per the calculations done in the previous chapter. These are summarized as follows:

- Input capacitor (C_{in}) = 470\mu F with ESR of 0.067\Omega
- Output Capacitor (C_{out}) = 120\mu F with ESR of 0.03\Omega
- Output Inductor (L_{out}) = 47\mu H with a dc resistance of 0.125\Omega

The input dc voltage is 12V, on-state drain to source resistance (R_{DSon}) of the MOSFETs is chosen as 45m\Omega, forward voltage drop of the diode is chosen as 0.4V, switching frequency is 200 kHz, duty ratio is 0.4166 to get the desired output dc voltage (Vo) of 5V and the load resistor is chosen as 5\Omega to get the desired output dc current (Io) of 1A. The simulation time chosen is 20 ms and the step size chosen is equal to one hundredth of the switching frequency, i.e., 0.05\mu s.

5.2 Conventional Buck Converter Simulation Results
The output voltage equals 4.627 V and output current is 0.9254 A. The output power is 4.282 W. The related waveforms obtained from the simulation are shown as follows.

From the waveforms shown in Fig. 5.4, it is clear that the converter is operating in the continuous conduction mode.
5.3 Synchronous Buck converter Simulation Results

The output voltage \( V_o \) obtained from the synchronous topology is 4.849 V; output current \( I_o \) is 0.9697A and the output power is 4.702W. The related waveforms obtained from the simulation are as shown.

![Gate pulses for the main MOSFET S and the synchronous MOSFET S1](image)

![Output Voltage of the Synchronous Buck converter](image)

![Output Current of the Synchronous Buck Converter](image)

![Voltage across and current through the inductor for synchronous topology](image)

The waveforms in Fig 5.11 clearly show that the synchronous buck converter is operating in the continuous conduction mode of operation.

![Current through and Voltage](image)

![Current through and voltage](image)
6. Conclusion
The design of both the converters is proper for operation in the continuous conduction mode. Also there is an increase in the output power with the synchronous buck converter topology as compared to the conventional buck converter topology keeping the duty ratio same for both the converters.

References